UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/833,653	04/13/2001	Shingo Kamitani	0033-0707P	1738

2292 7590 05/03/2005

BIRCH STEWART KOLASCH & BIRCH
PO BOX 747
FALLS CHURCH, VA 22040-0747

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/833,653	KAMITANI ET AL.	
	Examiner	Art Unit	
	Daniel Pan	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-17,19 and 20* is/are rejected.

7)☒ Claim(s) *10 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-20 are presented for examination.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1 , 6-9, 12-13, 17, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Yumoto (5,640,525).

3. As to claim 1, Yumoto discloses an execution control apparatus of a data driven information processor, wherein a handled instruction includes N+2 (N is an arbitrary integer of at least 1) inputs, and the inputs is a constant when an instruction has N+2 inputs', Yumoto uses 1 or z-inputs for instructions as shown in column 10, lines 43-45. Since the claim reads that N+2 inputs , this means a minimum of 3 inputs at most with N=1. Therefore, Yumoto's 1 and 2 input scheme meets the Imitation N+2 inputs.

Yumoto also taught :

a) outputs the number of inputs required for said instruction', Column 3, lines 27-31 shows that the packet is analyzed by an instruction execution packet detection unit (decoder) and it is determined whether the instruction is a 1 or z-input an instruction decoder that decodes an instruction in an input packet and instruction. It is shown here that a flag indicating the result of this determining (the number of inputs) is output.)

b) a waiting storage region including at least : a waiting data storage region that can store N waiting data in each waiting data address, and a data valid flag storage region indicating whether that stores a data valid flag for each waiting data address, said data valid flag indicating whether the N waiting data stored in said each waiting data address is respectively valid or invalid; (Column 4, lines 16-22 and figures 1 1 and 12 show a matching memory (waiting storage region) that stores data at addresses that includes a region (PRE flag) that indicates whether the data is valid or invalid. Since any integer greater than or equal to one, with N equal to one, each address has a corresponding piece of data.), a constant storage device including a region that stores a constant, and a constant valid flag storage region that stores a constant valid flag representing whether a constant stored in each constant address is valid or invalid', (Column 6, lines 32-40 and figure 20 show a constant data memory (storage device) that stores constant data with a region for storing a valid flag that tells if each constant is valid or invalid.), a constant readout unit that accesses said constant storage region according to the constant address information included in the input packet to read out a constant and a constant valid flag from a relevant address in said constant storage region (Column 6, lines 32-40)', a waiting operation determination unit (column 7, lines 1 1-12, data pair generation mechanism: interleave flag, address generation circuit, and data select circuit) that determines a hash address by a hash calculation from contents of the input packet', The address generation circuit inherently generates or determines an address. Column 4, lines 5-9 show that data from memory and the packet are checked for hash collision. This means that addresses for both the memory and packet data must be

generated by a hash calculation and thus a hash calculation is made for and thus from the input packet.) selects one predetermined way out of a plurality of predetermined ways of processing waiting data; (Column 7, lines 10-26 show that a selected data pair generation mechanism (out of a plurality) manipulates or processes the input data for generation of other data.), outputs a select signal for the predetermined ways of processing waiting data depending upon a combination of a data valid flag for said determined hash address, a constant valid flag read out by said constant readout unit, and the number of instruction inputs output from said instruction decoder for said waiting data storage region', (Column 4, lines 24-35 show that a packet is output based on the number of inputs and a valid flag for data from the matching memory (addressed by hash address and synonymous with the waiting data region as shown previously). Column 1 1, lines 44-47 shows that the selection is based off of a VLD flag (shown in column 10, lines 20-22 to be the valid flag of the constant) as well. Column 4, lines 31-35 show that the valid data flag (PRE) is updated) and updates the data valid flag for said hash address based on the select predetermined way of processing waiting data; (Column 4, lines 31-35 show that the valid data flag (PRE) is updated.) and a waiting region access unit being responsive to said selected signal to implement a waiting process corresponding to said select signal. (Column 7, lines 20-26, shows a data select circuit (waiting region access unit) operates the said mechanisms from above based on the token received from the unit above.)

4. As to claim 6, Yumoto discloses the apparatus according to claim 1, wherein N of said data valid flags are prepared for one address (Figure 1 1 and 12 show that the data valid flags (PRE flags) are prepared for one address.).

5. As to claim 7, Yumoto discloses the apparatus according to claim 6, wherein address', (Figures 1 1 and 12 show that each PRE flag associated with one each data valid flag is prepared of one bit for one waiting data of one address. As shown above, the PRE flag indicates whether data is valid (PRE=1) or invalid (PRE=0) and as can be noted from the rest of Yumoto's disclosure, these are the only two values of this flag. Thus the valid flag is one bit.), and said data valid flag storage region includes N flip-flop circuits for each address, each flip-flop circuit storing a data valid flag of one bit. (Figures 9 and 29 show the matching memory (waiting data storage region), 284. The figures show the memory to have D inputs (DI) and outputs (DQ) for a specified address given on the A input. One of ordinary skill in the art would recognize this to mean that the storage area comprises D flip-flops for each address. Since each address has one valid flag associated with it, each flag is stored in a D flip-flop.)

6. As to claim 8, Yumoto discloses the apparatus according to claim 1, wherein said data valid flag storage region includes an erasable storage circuit that clears the region in response to a reset signal. (Column 4, lines 10-19 show that the valid flag is invalidated or cleared to zero. This means that there is an erasable storage circuit that performs this function. Since this updating or clearing is only done at a certain point, it is response to a signal, which can be called a reset signal.).

7. As to claim 9, Yumoto discloses the apparatus according to claim 8, wherein each of data valid flag is prepared of one bit for one waiting data of one address, and said erasable storage circuit includes a D flip-flop circuit for each address, each D flip-flop circuit storing a data valid flag of one bit. (As shown above, the PRE flag indicates whether data is valid (PRE=1) or invalid (PRE=0) and as can be noted from the rest of Yumoto's disclosure, these are the only two values of this flag. Thus the valid flag is one bit. Figures 9 and 29 show the matching memory (waiting data storage region), 284. The figures show the memory to have D inputs (DI) and outputs (DQ) for a specified address given on the A input. One of ordinary skill in the ad would recognize this to mean that the storage area comprises D flip-flops for each address. Since each address has one valid flag associated with it, each flag is stored in a D flip- flop-) wherein N=1. With N=1 , a handled instruction has at most 3 inputs and the waiting data.

8. As to claim 12, Yumoto discloses the apparatus according to claim 1, storage holds 1 piece of data for each address. (As described above, the disclosure of Yumoto has 1 and 2 inputs which meets the limitation of at most 3 inputs. Also as shown above and in figures 1 1 and 12, address holds one piece of data.)

9. As to claim 13, Yumoto discloses an execution control method of a data driven information processor, wherein a handled instruction includes N+2 (N is an arbitrary integer of at least 1) inputs, and one of the inputs is a constant when an instruction has N+2 inputs, said data driven information processor comprising: (Yumoto uses 1 or z-inputs for instructions as shown in column 10, lines 43-45. Since the claim reads that

N+2 inputs at most, this means a minimum of 3 inputs at most with N=1. Therefore, Yumoto's 1 and 2 input scheme meets the limitation of at most N+2 inputs. Also being taught are : an instruction decoder that decodes an instruction in an input packet to output the number of inputs required for said instruction', Column 3, lines 27-31 shows that the packet is analyzed by an instruction execution packet detection unit (decoder) and it is determined whether the instruction is a 1 or z-input instruction. It is shown here that a flag indicating the result of this determining (the number of inputs) is output.) a waiting storage region including a waiting data storage region that can store N waiting data in each waiting data address, and a data valid flag storage region that stores a data valid flag for each waiting address, said data valid flag indicating whether the N waiting data stored in said each waiting data address is respectively valid or invalid id ; (Column 4, lines 16-22 and figures 1 1 and 12 show a matching memory (waiting storage region) that stores data at addresses that includes a region (PRE flag) that indicates whether the data is valid or invalid. Since is any integer greater than or equal to one, with N equal to one, each address has a corresponding piece of data.), and a constant storage device including a region that stores a constant, and a constant valid flag storage region that stores a constant valid flag representing whether a constant stored in each constant address is valid or invalid', (Column 6, lines 32-40 and figure 20 show a constant data memory (storage device) that stores constant data with a region for storing a valid flag that tells if each constant is valid or invalid.), and a constant readout unit accessing said constant storage region with a node number of the input packet as a constant address to read out a constant and a constant valid flag from a

relevant constant address in said constant storage region (Column 6, lines 32-40)*, and a waiting operation determination unit (column 7, lines 1 1-12, data pair generation mechanism: interleave flag, address generation circuit, and data select circuit) that determines a hash address by a hash calculation from contents of the input packet, The address generation circuit inherently generates or determines an address. Column 4, lines 5-9 show that data from memory and the packet are checked for hash collision. This means that addresses for both the memory and packet data must be generated by a hash calculation and thus a hash calculation is made for and thus from the input packet.), and selects one predetermined way out of a plurality of predetermined ways of processing waiting data, col. 7, lines 10-26 show that a selected data pair generation mechanism (out of a plurality) manipulates or processes the input data for generation of other data.), and outputs a select signal for the predetermined way of processing waiting data corresponding to a combination of a data valid flag for said determined address, a constant Valid flag read out by said constant readout unit, and the number of instruction inputs output from said instruction decoder for said waiting storage region, Column 4, lines 24-35 show that a packet is output based on the number of inputs and a valid flag for data from the matching memory (addressed by hash address and synonymous with the waiting data region as shown previously). Column 1 1, lines 44-47 shows that the selection is based off of a VLD flag (shown in column 10, lines 20-22 to be the valid flag of the constant) as well. Column 4, lines 31-35 show that the valid data flag (PRE) is updated.) and updating the data valid flag for said hash address based on the selected predetermined way of processing waiting data; (Column 4, lines 31-35

show that the valid data flag (PRE) is updated.) and a waiting region access unit being responsive to said select signal to implement a waiting process corresponding to said select signal', (Column 7, lines 20-26, shows a data select circuit (waiting region access unit) operates the said mechanisms from above based on the token received from the unit above, and decoded by said instruction decoder, and the number of inputs required by the instruction is output', (Column 3, lines 27-31 shows that the packet is analyzed by decoding an instruction, wherein an instruction in the input packet is an instruction execution packet detection unit (decoder) and it is determined whether the instruction is a 1 or z-input instruction.

It is shown here that a flag indicating the result of this determining (the number of inputs) is output.), and reading out a constant, wherein said constant storage region is accessed based on address information included in the input packet, and a constant and a constant valid flag are read out from a relevant constant address in said constant storage region', (Column 6, lines 32-40 shows all of this including that address information is gotten from the destination information of the instruction token.) determining a waiting process, wherein an hash address is determined by hash calculation from contents in the input packet; (Column 7, lines 1 1-12 show an address generation circuit for determining an address. Column 4, lines 5-9 show that data from memory and the packet are checked for hash collision. This means that addresses for both the memory and packet data must be generated by a hash calculation and thus a hash calculation is made for and thus from the input packet, and one predetermined way out of a plurality of predetermined ways of processing waiting data is selected,

(Column 7, lines 10-26 show that a selected data pair generation mechanism (out of a plurality) manipulates or processes the input data for generation of other data.), and a select signal for the predetermined way of processing waiting data is output corresponding to a combination of a data valid flag for said determined hash address, a constant valid flag read out from said constant readout unit, and the number of instructions output from said instruction decoder for said waiting storage region', (Column 4, lines 24-35 show that a packet is output based on the number of inputs and a valid flag for data from the matching memory (addressed by hash address and synonymous with the waiting data region as shown previously). Column 1 1, lines 44-47 shows that the selection is based off of a VLD flag (shown in column 10, lines 20-22 to be the valid flag of the constant) as well. Column 4, lines 31-35 show that the valid data flag (PRE) is updated.), and the data Valid flag is updated corresponding to the hash address based on the selected predetermined way of processing way of processing data', (Column 4, lines 31-35 show that the valid data flag (PRE) is updated.). And executing the waiting process, wherein, in response to said select signal, a waiting process corresponding to said select process is performed. (Column 7, lines 20-26, shows a data select circuit (waiting region access unit) operates the said mechanisms from above based on the token received from the unit above.)

10. As to claim 17, Yumoto discloses the apparatus according to claim 13, wherein said data valid flag storage region includes an erasable storage circuit clearing

the region in response to a reset signal, said method further comprising the step of applying a reset signal to said storage circuit, thereby clearing said data valid flag storage region. (Column 4, lines 10-19 show that the valid flag is invalidated or cleared to zero. This means that there is an erasable storage circuit that performs this function. Since this updating pr clearing is only done at a certain point, it is in response to a signal, which can be called a reset signal.).

11. Claims 2-5 and 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto in view of Choquette (6,530,011).

12. As to claim 2, limitations of claim 1 already discussed in previous paragraph, therefore, it will not be repeated herein. Yumoto does not disclose the apparatus wherein said constant storage region includes a first constant storage region that stores constant data of a first type, and a second constant storage region that stores constant data of a second type, wherein said constant readout unit identifies whether the readout constant is of said first type or said second type according to the address. Yumoto does disclose, as shown above, a constant readout for reading constant values from a constant storage region.) . Choquette has disclosed a constant storage region including a first constant storage region that stores constant data of a first type, and a second constant storage region that stores constant data of a second type; (Column 4, lines 62-65 show a register file (constant storage region) that contains two sets of register banks (first and second constant storage region) that holds two different types of constant data, vector and scalar data. Since the constant readout unit disclosed by Yumoto reads

the constant data out from the constant storage region, when the dual-type constant storage region of Choquette is used with the disclosure of Yumoto, this constant readout unit it would inherently identify whether a constant is of the first type or second type (according to the register bank and thus the address) since, as shown in column 1, lines 16-24 of Choquette, the two types are represented differently and treated differently.). Choquette has shown in column 1 , lines 43-46 using vectors improves system performance for data accesses and computations. his improved performance would have motivated one of ordinary skill in the art to modify Yumoto to use vectors and store them in the manner disclosed by Choquette.

13. It would have been obvious to one of ordinary skill in the: art at the time of invention to modify the design of Yumoto to include the use of vectors and store them in the manner disclosed by Choquette so that system performance is improved.

14. As to claim 3, Yumoto in view of Choquette has disclosed the apparatus according to claim 2, wherein said constant data of the first type is a scalar constant, and said constant data of the second type is a vector constant, as shown above.

15. As to claim 4, Yumoto in view of Choquette has disclosed the apparatus according to claim 3, wherein each input packet can store plurality of data, and said waiting operation determination unit can store a plurality of data for each packet. (Figures 14 and 15 show the format of data packets (column, 9, lines 10-13) and it can be seen that the data packets store a plurality of data via each field in the packet. Since no type or use of the data was specified in the claim, this is sufficient to meet this data

limitation of the claim. Column 6, lines 66-67 shows that the above described matching memory, which stores a plurality of waiting data for the packets, is included with the data pair generation mechanisms (waiting operation determination unit.)

16. As to claim 5, Yumoto in view of Choquette as cited above, disclosed the apparatus according to claim 2, wherein said constant data of the first type is a scalar constant of a first length, and said constant data of the second type is a constant of a second length different from said first length. (Figure 3, shows that the double precision scalar data is if a different length than the single precision vector data.), and the constant data of the second type is a scalar constant of a second length different from said first length.

17. Yumoto in view of Choquette, as described above, does not disclose the Choquette does disclose, as seen in figure 3, a second scalar constant C. type of a double precision word length, and single and double precision data interchangeably when necessary. This allows Choquette has shown in column 8, lines 28-33 that calculations use both for great flexibility in the type of calculations that may be performed since two data types are used. This flexibility of execution would have motivated one of ordinary skill in the art to modify the design of Yumoto in view of Choquette to include the use of two scalar data types of different lengths as taught by Choquette. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Yumoto in view of Choquette to include the use of two different scalar data types and lengths as taught by Choquette so that greater flexibility in execution is attained.

18. As to claim 14, Yumoto discloses the method according to claim 13, Yumoto does not disclose the method wherein said constant storage region includes a first constant storage region that stores constant data of a first type, and a second constant storage region that stores constant data of a second type, wherein said step of reading out a constant includes the steps of:

a) determining whether the readout constant is of said first type

or said second type based on the address, and reading out the constant.

19. Yumoto does disclose, as shown above, a constant readout unit for reading constant values from a constant storage region, and Choquette has disclosed a constant storage region including a first constant storage region that stores constant data of a first type, and a second constant storage region that stores constant data of a second type; (Column 4, lines 62-65 show a register file (constant storage region) that contains two sets of register banks (first and second constant storage region) that holds two different types of constant data, vector and scalar data. Since the constant readout unit disclosed by Yumoto reads the constant data out from the constant storage region, when the dual-type constant storage region of Choquette is used with the disclosure of Yumoto, this constant readout unit it would inherently identify whether a constant is of the first type or second type (according to the register bank and thus the address) since, as shown in column 1 , line 16-24 of Choquette, the two types are represented differently and treated differently.), and Choquette has shown in column 1, lines 43-46 that using vectors improves system performance for data accesses and computations.

This improved performance would have motivated one of ordinary skill in the art to modify Yumoto to use vectors and store them in the manner disclosed by Choquette. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Yumoto to include the use of vectors and store them in the manner disclosed by Choquette so that system performance is improved.

20. As to claim 15, Yumoto in view of Choquette has disclosed the method according to claim 14, wherein said constant data of the first type is a scalar constant, and said constant data of the second type is a vector constant, as shown above.
26. As to claim 16, Yumoto disclosed the apparatus according to claim 14, wherein said constant data of the first type is a scalar constant of a first length, and said constant data of the second type is a constant of a second length different from said first length. (Figure 3, shows that is if a different length than the single precision the double precision scalar data a vector data.), and a method wherein said constant data of the second type is a scalar constant of a Yumoto in view of Choquette, as described above, does not disclose the second length differing from said first length. However, Choquette does disclose, as seen in figure 3, a second scalar constant type of a double precision word length.
21. Choquette showed in column 8, lines 28-33 that calculations use both single and double precision data interchangeably when necessary. This allows for great flexibility in the type of calculations that may be performed since two

data types are used. This flexibility of execution would have motivated one of Ordinary Skill in the art to modify the design of Yumoto in view of Choquette to include the use of two scalar data types of different lengths as taught by Choquette. It would have been obvious to one of ordinary skill in the ad at the time of invention to modify the design of Yumoto in view of Choquette to include the use of two different scalar data types of lengths as taught by Choquette so that greater flexibility in execution is attained.

22. Claims 1 1 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yumoto in view of Hennessy.

23. As to claim 1 1 , Yumoto discloses the apparatus according to claim 13, and to the extent wherein N=2. With N=2, a handled instruction has at most 4 inputs and the waiting data storage holds 2 pieces of data for each address. As described above, the disclosure of Yumoto has 1 and 2 inputs which meets the limitation of at most 4 inputs.

24. Yumoto does not disclose that 2 pieces of data are stored for each address in the waiting data storage region as is the case when N=2. It is shown that multiple reads or writes occur with this type of memory design.

25. An address is sent to multiple banks where the multiple stored data is manipulated. Therefore, a memory storage system is disclosed that describes Hennessy teaches on pages 429-431, a manner of interleaving memory. storing two pieces of data for each address.

26. The ability to read or write multiple words at a time gives a performance boost that would have motivated one of ordinary skill in the art to modify the design of Yumoto to include the memory interleaving design disclosed by Hennessy. It would have been obvious to one of ordinary skill in the ad at the time of invention to modify the design of Yumoto to include the interleaved memory design taught by Hennessy so that memory performance may be increased.

27. As to claim 19, wherein N=2. With N=2, a handled instruction has at most 4 inputs and the waiting data storage holds 2 pieces of data for each address. As described Yumoto discloses the method according to claim 1, and to a certain extent above, the disclosure of Yumoto has 1 and 2 inputs which meets the limitation of at most 4 inputs.

28. Yumoto does not disclose that 2 pieces of data are stored for each address in the waiting data storage region as is the case when N=2. Hennessy teaches on pages 429-431, a manner of interleaving memory. It is shown that multiple reads or writes occur with this type: pf-memory design. An address is sent to multiple banks where the multiple stored data is manipulated. Therefore, a memory storage system is disclosed that describes storing two pieces of data for each address.

29. The ability to read or write multiple words at a time gives a performance boost that would have motivated one of ordinary skill in the art to modify the design of Yumoto to include the memory interleaving design disclosed by Hennessy. It would have been obvious to one of ordinary skill in the art at the time of invention to modify the

design of Yumoto to include the interleaved memory design taught by Hennessy so that memory performance may be increased.

30. The following is the response by examiner to applicant's remark on 04/06/05 :

31. Applicant argued that the hash collision detection unit that the Fc-adapted z-input instruction execution packet detection unit of Yumoto et for generating a flag indicating whether an input packet is a z-input instruction execution or not merely determines the presence of a z-input instruction execution and is not analogous to "a handled instruction that includes N + 2 (N is an arbitrary integer of at least 1) inputs, in which one of the inputs is a constant when an instruction has N + 2 inputs." Yumoto et al. merely detects whether an input packet is argument data of a 1- input or z-input instruction. Moreover, there is nothing in the invention of Yumoto et al. that discloses an instruction that includes more than 2 inputs. In the present invention, the handled instruction includes N+2 inputs, where N is an arbitrary integer of at least 1, which will result in more than 2 inputs.

32. As to the applicant' remark above, Yumoto taught the detection of whether an input packet is argument data of a 1- input or z-input instruction, yumoto also discloses an execution control apparatus of a data driven information processor, wherein a handled instruction includes N+2 (N is an arbitrary integer of at least 1) inputs, and the inputs is a constant when an instruction has N+2 inputs', Yumoto uses 1 or z-inputs for instructions as shown in column 10, lines 43-45. Since the claim reads that N+2 inputs ,

this means a minimum of 3 inputs at most with N=1. Therefore, Yumoto's 1 and 2 input scheme meets the limitation N+2 inputs. Therefore, Yumoto did disclose the instruction that includes more than 2 inputs, and the handled instruction includes the N+2 inputs, where N is an arbitrary integer of at least 1 (see example of N=1 discussed above) , which resulted in more than 2 inputs.

36. Claims 10 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. When the number of inputs is N+2, this means that the number of inputs is 3 or more depending on N. The prior art of record does not specifically teach a dataflow processor where when the number of inputs is 3 or more, the constant flag is set to an invalid state and the number of instruction inputs is set to N+1 where these new values are then output to the waiting processing unit. In addition, no prior art of record suggests that it would have been obvious to one of ordinary skill in the ad at the time of invention to modify the prior ad of record wherein when the number of inputs is 3 or more, the constant flag is set to an invalid state and the number of instruction inputs is set to N+1 where these new values are then output to the waiting processing unit.

33. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Iwashita et al. (4,594,653) is cited for the teaching of the memory for storing the constant (see col.9, lines 7-25).

34. Yumoto (5,640,525), Choquette (6,530,011), Hennessy were already cited to applicant on the record , therefore, copies are not included herein.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696, or the new number 571 272 4172. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712, or the new number 571 272 4162. The fax phone number for the organization where this application or proceeding is assigned is 703 306 5404.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

21 Century Strategic Plan

DANIEL H. PAN
PRIMARY EXAMINER
GROUP